PerfectVIPs
Right Tools... Perfect Chip

ETHERNET 10M/100M/1G/10G/40G/100G VIP

GENIE-ETH™

ETHERNET VERIFICATION IP

OVERVIEW

The **Genie-ETH** Verification Products are the industry's most comprehensive verification solution for Ethernet based designs. The intelligent **Verification Engine**, integrated **Interface monitor** and comprehensive **checkers and scoreboards** provide Perfect combination of test cases and environment to ensure first silicon success.

The **Genie-ETH VIP** provides a quick and efficient way to verify any Ethernet based design - **MAC** or **PHY**. The VIP will automatically generate transactions and respond to bus activity, inject errors at any point, verify protocol compliance via checker and view violations via report generator. Genie-ETH provides a complete verification solution based upon SystemVerilog and UVM methodology.

FEATURES

- Compliant to IEEE Std 802.3™ Specification, IEEE Std 802.3ba
- Station management registers can be accessed via MDIO interface or test interface
- Fully configurable error generation with the help of knobs (protocol errors and packet errors) allows testing of error detection mechanisms under realistic scenarios
- Simple yet extremely powerful test interface allows control over all aspects of VIP behaviour and promotes re-use of test code
- Supports auto-negotiation and synchronization
- FEC support for speeds exceeding 10G.
- Supports multiple instantiations of agents for generating and collecting Ethernet packets
- Pre built sequence libraries for extensive scenario generation and corner case tests
- Supports configuration of different ports independently
- Configurable log file with test statistics - data path and station management
- Supports all interfaces for data rates from 10Mbps to 100G
- Monitors protocol and reports violations
- Supports frame types – MAC data and Control Pause
- Ability to extend the coverage points library - user defined
- Scoreboard provisioning
- Supports half and full duplex mode
- Automatic generation of CRC and padding
- Active or passive BFM modes
- Generation of random Interpacket gap
- Full CSMA/CD support
- Enable/Disable capabilities of Checker, Scoreboard, and Coverage modules
- Comprehensive mechanism for trace/debug of VIP behavior
- Automated packet generation in each layer
- Supports OVM and UVM

Supported Ethernet Interfaces and Network Layers

10/100 Mbps--MII,SMII,CSMA/CD, Full Duplex and flow control, RMII, & MDIO

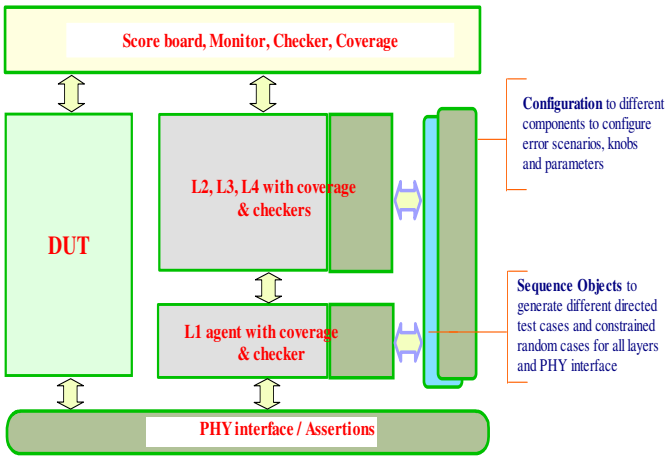
1Gbps--GMII, QSGMII , RGMII, SGMII, Auto-negotiation ,& MDIO

10Gbps--10G-Base, KRXGMII, XTBI ,XAUI ,10G-Base-KX4, FEC ,& Auto-negotiation

40Gbps--40G-Base, KR4XLGMII,40G-Base-CR4 FEC, & Auto-negotiation

100Gbps--100G-Base,KR10CGMII,100G-Base-CR10,100G-Base-LR4,Auto-negotiation,& FEC

L2 layer--VLAN (502.1Q), QinQ (Stacked VLAN),VPLS/MPLS, & ARP
L3 layer -IPV4 & IPV6
L4 layer-TCP,UDP, ICMP, Tunnel SCTP on UDP



DATASHEET
Rev. 1.2

PRODUCT DETAILS

Verification Engine

Genie-Eth is configurable so users can focus on any part of their design. Enriched with knobs to provide complete control over packet transmission and reception behaviour, it contains simple and easy to use APIs/sequences to inject packet errors, protocol related errors and collision scenarios. It also enables management read and writes.

L3 and L4 Packet Generators

This module allows the user to generate L4 and L3 packets which can be used as input to the DUT via the Ethernet MAC VIP.

MAC Design (NIC Card)

When the DUT is a MAC layer entity, the VIP is configured as a PHY layer entity connected through a PHY interface. It initiates transactions on the reception lines to verify the MAC logic.

PHY Design (NIC Card)

When the DUT is a PHY layer entity, the VIP is configured as a MAC layer entity connected through a PHY interface. It initiates transactions on the transmission lines to verify the PHY logic.

Multiple MAC/PHY Design (Switch/Repeater)

When testing a design with multiple MACs and PHYs, multiple instances of the MAC and PHY VIP will need to be configured. This provides the ability to test and analyze each port independently.

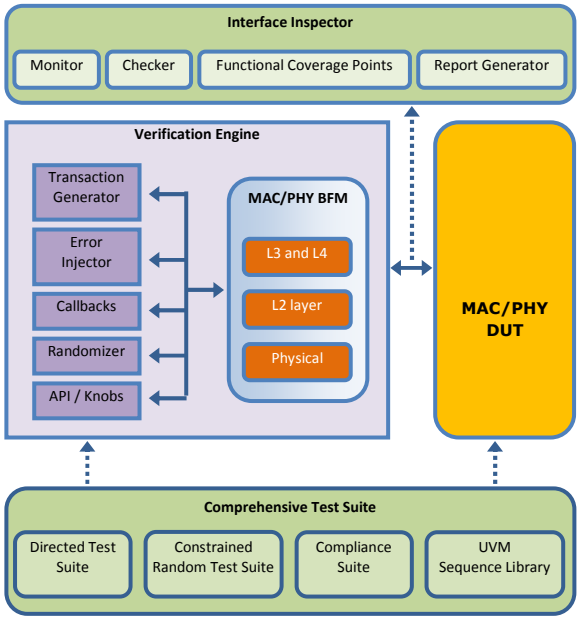


Fig. 2: Ethernet Verification Environment

Interface Inspector:

The Interface Inspector tracks the traffic on the interface and provides protocol and packet checking capability. It supports user-configured watch points to trigger activity based on specific model and bus events. Functions can be enabled and disabled individually for a particular test. It generates log files and displays packet transmission information. The log files can be tailored to extract specific information to expedite the debugging process.

Supported simulators: Aldec Cadence Mentor Synopsys

ETHERNET COMPLIANCE SUITE	ETHERNET SOLUTIONS
Developed by PerfectVIPs to thoroughly exercise Ethernet designs, the compliance suite is a comprehensive verification test suite that provides many test cases. ▪ Verifies all aspects of Ethernet designs ▪ Provides comprehensive design coverage targeted at 10Mbps to 100Gbps and management interface ▪ Identifies all protocol violations ▪ Provides detailed reports on functional coverage ▪ Provides directed and constrained-random regression testing capability ▪ Developed with actual customer designs	Developed by PerfectVIPs to address different system level Ethernet architectures, the following solutions are available. Verification IP: ▪ Ethernet MAC VIP ▪ Ethernet PHY VIP ▪ Ethernet MAC/PHY VIP (configurable) ▪ Ethernet MAC+PCS VIP for 10M/100M, 1G, 10G , 40G and 100G ▪ Ethernet L3+L4+VIPs listed above

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